REMARKS

In accordance with the foregoing, claims 11-16, 18, 19, 23 and 24 have been amended and new claim 25 has been added. Claims 11-25 are pending and under consideration.

In item 1 of the Office Action, the Examiner raises various claim objections. The Examiner's careful review of the claims is gratefully appreciated. The claims have been amended to address the issues raised by the Examiner, where appropriate. A portion of the Examiner's suggestions have not been followed. For example, the meaning of claim 12 would be altered if "in each case" were deleted.

For item 2 of the Office Action, Applicants disagree with the Examiner's assertion that claims 13 and 15 are duplicates and claims 14 and 16 are duplicates. Claims 13 and 14 relate to a partition, whereas claims 15 and 16 relate to all partitions.

In item 4, claims 11 and 24 are rejected under 35 U.S.C. § 112, second paragraph. To address this objection, claims 11 and 24 have been amended to recite a chargeable dynamic element.

In item 5, claim 12 is rejected under 35 U.S.C. § 112, second paragraph. To address this rejection, claim 12 has been amended to recite "a predetermined potential."

Beginning on page 4 of the Office Action, claims 11-24 are rejected under 35 U.S.C. § 103(a) as being obvious over the Ulrich Bretthauer et al. paper (the Bretthauer paper) entitled BRASIL: The Braunschweig Mized-Mode-Simulator for Integrated Circuits in view of the H. Spiro paper (the Spiro paper) entitled Simulation of Integrated Circuits. The Bretthauer paper discloses a timing simulator for digital MOS circuits, whereby a modeling of the drain-source-channel of transistors with time variable conductance leads to a linear time-variant RC-network. The capacitances which are summed are the parasitic capacitances of the transistors and the capacitances associated with each node. In the Bretthauer paper, see the abstract and text spanning from the last paragraph of page 2 to the first paragraph of page 3.

Independent claims 11 and 24 have been amended to recite "adding a chargeable dynamic element at each node of the circuit." Antecedent basis for this claim change can be found, for example, at paragraph [0020] of the original application and at Fig. 1, step 3. As described in the specification, a chargeable dynamic element is added to each node of the circuit in connection with using a charging method for the parallel calculation of the set point of individual partitions of an electrical circuit. New claim 25 is more specific than claims 11 and 24 and recites that an equal capacitance is provided at each node of a partition. Claim 25 is based

on claims 11 and 13.

In the Bretthauer paper, there is no suggestion for adding a chargeable dynamic element in connection with a charging method for parallel calculation of individual partitions of an electrical circuit. The Bretthauer paper states that the circuit elements at the borders of the partitions have to be modeled with network elements. In this modeling process, the gates of MOS transistors in the area of the simulation can be treated as constant capacitors. See page 1, column 2, second paragraph of the reference. The value of each constant capacitor is the sum of the parasitic capacitances of the transistor and all capacitances tied to the node. As mentioned above, there is not an additional dynamic element provided for use in a charging method for parallel calculation of individual partitions an electrical circuit, as claimed.

The Examiner cites the Spiro paper, asserting that it would have been obvious to combine the teachings of the references "to achieve rapid and accurate convergence." It is unclear where the Examiner obtains this alleged motivation for the combination. In fact, it appears that there is no motivation to combine the references.

Even if the Spiro paper were combined with the Bretthauer paper, the claimed invention would not result. Specifically, the Spiro paper does not disclose or suggest adding a dynamic charging element at each node of the circuit in connection with a charging method for the parallel calculation of individual partitions of an electric circuit. The Bretthauer paper simply teaches to simulate the gates of MOS transistors in the area as constant capacitors.

With regard to new independent claim 25, this claim additionally recites that an equal capacitance is provided at each node of a partition as the chargeable dynamic elements. The Bretthauer paper only discloses that the capacitance at a node is the sum of the parasitic capacitance of the transistor and all capacitances tied to the node. This capacitance is by no means equal at each node. That is, the capacitance would vary depending on the different gate structures and connected circuits. In addition to the reasons described above with regard to claims 11 and 24, claim 25 distinguishes over the references because of the equal capacitance limitation.

In view of the above, it is submitted that the prior art rejection should be withdrawn.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: Jan 9 2004

By: Mark J. Henry
Registration No. 36,162

1201 New York Avenue, NW, Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501

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STAAS & HALSEY
By: Margaret Fry
Date: 1-9-04